Improvement Silicon Nanostructured Surface by Laser Induced Etching Process

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Abstract

Surface reconstruction of silicon using lasers could be utilized to produce silicon nanostructures of various features. Electrochemical and photoelectrochemical etching processes of silicon were employed to synthesize nanostructured surface. Effects of current densities 5, 10 and 20 mA/cm2 on the surface features were examined. It is found that the surface porosity and layer thickness increase with the current density. Moreover, large surface area of 410 m2/cm3 can be achieved when laser power density of 0.6 W/cm2 was used during the etching process. Optimum operating conditions were found to achieve better silicon nanostructured surface features. The surface roughness can be reduced to 8.3 nm using laser beam of 650 nm irradiated the silicon surface during the photoelectrochemical etching process. The surface morphology of the nanostructured silicon surface using SEM and AFM could give rich details about the surface. Silver nanoparticles of 10 – 20 nm was embedded at the nanostructured silicon surface by LIFT process to reduce the surface resistance and maintain the large surface area. This technique enables silicon nanostructures to be efficiently used in many optoelectronic applications.

Keywords: Silicon Nanostructure, Porous Silicon, LIFT, Silver Nanoparticles.

1. Introduction

Nanotechnology is a design, manipulation and constructing materials for applications by controlling the size, shape and properties at less than 100 nm. New materials and new-engineered surfaces could enable products for better performance **[1].**

Considerable progress using lasers has been achieved in the science of production nanoparticles and nanotechnologies. In some applications, the laser beam is preferable to be used in nanotechnology due to the unique characteristics of the laser beam, such as spatial and temporal coherence [2].

The laser surface engineering is one way to improve the surface properties of materials. Laser surface engineering encompasses several applications that are mainly related to enhancing one of the surface dependent properties such as hardness, friction, fatigue and resistance to wear, corrosion, etc. [3].

The main advantage of laser as a material treatment tool is the ability to precisely control its position and at the rate that energy deposited. This control is exercised by selecting the correct laser treatment parameters to achieve the desired modification of the material. Modifying the surface properties on multi-length scales plays an important role to improve the material's performance for a given application. For example, the surface cosmetic appearance and its absorption properties can be controlled by changing its texture [4]. The exposure of the material to wear and surface damage can be reduced by changing the surface chemistry, morphology, and crystalline structure [5]. Also, one can consider the frictional, adhesive, and wet forces acting on a material interface severely affected by the size and shape of existing micro and nanoscale features [6]. As such, multi-band surface modifications are critical to the development of new material structures and to the engineering of detailed interactions that occur at surfaces and facades [7]. Various mechanisms could be employed to describe laser surface engineering of silicon [8-10].

Photoelectrochemical process utilizes Laser-assisted etching of silicon is considered as a relatively rare, preferable technique to produce for creating modified silicon nanostructures at the surface [11]. This technique has been extensively investigated for various semiconductors last two decades using a wide

variety of laser sources from low power CW laser to nanosecond laser pulse for a wide laser wavelength range from 0.4 to 10.6 μm [12]. This technique is widely used since it is applicable for all types of conductivities (intrinsic, n and p-type semiconductors), solar cells and sensors. The laser light can play a dual role in this process; initial the chemical reaction and define the etching direction [13,14]. Generally, in this process, chemical reaction takes place due to externally supplied holes and the fluorine ions of HF acid. While for EC etching process, the holes are supplied from an external power supply, these holes move toward the front of the silicon electrolyte interface and silicon dissolution takes place. Subsequently, pores are formed at the silicon surface and which produce porous structure consisting silicon nanostructures [15].

On the other side, large surface area for silicon nanostructures increase the surface resistance which limit some other optoelectronic applications such as light emitters and sensors [16-18]. Therefore, there was a great demand for nanostructured surfaces of large surface area and simultaneously, low resistance. Aim of this work is preparing silicon nanostructure of controllable feature including the large surface area and low resistance by embedding silver nanoparticles at the surface.

2. Experimental Procedure

Laser-induced etching is a very interesting process of forming silicon nanostructures at the silicon surface. At room temperature, both photoelectrochemical etching (PEC) and electrochemical etching (EC) can be used to prepare silicon nanostructures. In this work, EC and PEC processes are conducted with the following procedure; the silicon samples were cut with

dimensions of 2 cm^2, this area is suitable for the Teflon cell slot to enter the laser beam. Those samples were cleaned with ethanol to eliminate the oxide layer, and then dried. Then, these samples were put in the etching cell which made from Teflon. The Teflon material is chosen for its high resistivity to HF acid, interspersed with electrodes that are connected to the power supply. The front side of the wafer should face the platinum wire (the cathode) while the back side is connected to the stainless-steel anode. Using HF solution, one can use electrical current for EC and laser light with electrical current for PEC. The HF acid is diluted to concentration 20%, the irradiation time of the diode laser for PEC etching is 30 minutes and the etching time of EC etching is also 30 minutes.

Various parameters are varied in the experiments such as: wafer conductivity, laser wavelength, current density, laser power density. To study one of these parameters, the studied parameter should be varied while others kept constants, for each experiment, the surface structure and the porous layer thickness should be monitored.

Nd: YAG laser (Trumpf Co., Germany) with a pulse mode operation and varied energy in the range 0.5 to 6 J was employed in this work. The beam diameter was 3 mm and the divergence angle og 2 mrad. Fixed number of pulses and energy was used for Laser induced Forward Transfer (LIFT) process. High purity nano silver paste of 10 - 20 nm particle size was also employed in this process.

The electrical measurements were conducted by RLC multi-meter for frequencies 1 to 100 KHz. Aluminum film was deposited in a planner configuration for resistance measurements. Figure 1 illustrates the experimental set for the PEC process.
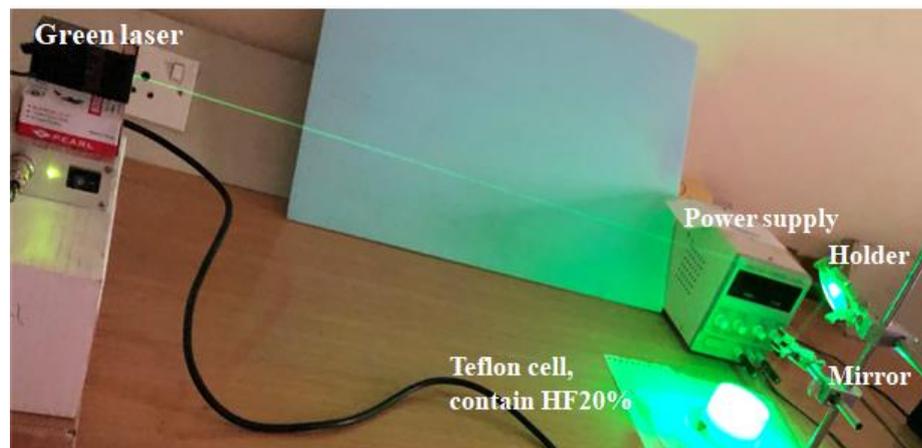

Figure 1: The Experimental set up for PEC etching process.

3. Results and Discussion

One of the most important and effective parameters for production of porous silicon in the PECE process is the wavelength of the laser used [19]. Each wavelength has a specific penetration depth within the silicon. Therefore, the thickness of the porous layer will vary from one wavelength to another. Three different wavelengths (red, green, violet) have been used with 100 mW. The rest of the

processing parameters such as the HF concentration of 20%, current density 20mA/cm^2, irradiation time 30 minutes and p-type silicon wafer are kept constant.

Figure (2) shows the porous layers produced by various laser wavelengths. In (a), the silicon structure appears in different pore shapes and sizes. It is also clear that the porous structure prepare by green laser (b) has a random distribution with different pore

diameters and the layer thickness is lower than in (a). In the sample that processed by the violet laser (c), the structure of porous silicon has very small depth. Due to the long wavelength of 650nm, thick layer of high pore is produced. While using wavelength 532nm, it was found that the thickness of the porous layer (60 μm) was lower than that of the red wavelength (100 μm) in terms of density and the pore dimensions due to the small penetration depth. While using short wavelength of 405nm, it is found that the thickness of the porous layer (20μm) is lower than in the two cases mentioned above, also the numbers of pores and their dimensions are very small.
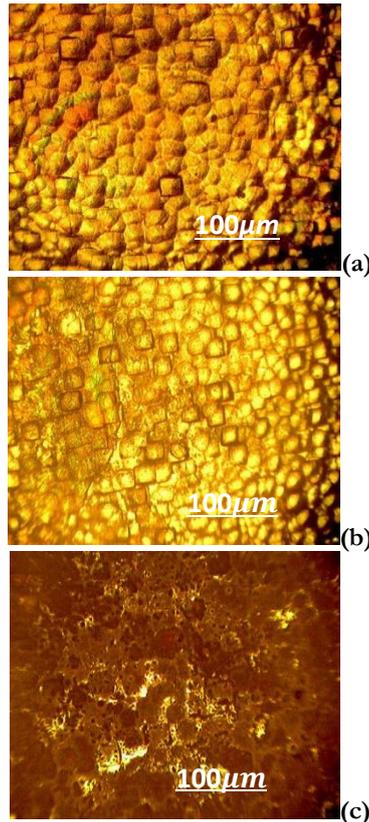
Figure 2: P-Si layer produced by PEC process using, a: red laser diode, b: green laser diode, c: violet laser diode.

To study effect of laser power density, the laser wavelength 650 nm was used and the rest of other parameters are kept constant (current density 20 mA/cm^2, irradiation time is 30min, HF acid concentration is diluted to 20%). It is noticed that at higher power density, the shape of the pores and their number becomes larger size of pore and lower number. When using laser power density of 0.4 W/cm^2, the chemical reaction begins and lead to reconstruct the surface. The pores were found to be too small, irregular and randomly distributed. While at higher power density of 0.6 W/cm^2 ,the chemical reaction increases and generate large numbers of electron-hole pairs which leads to generate extra holes. These holes arrive at surface for more dissolving of silicon wafer, also we found larger pores which have different shapes and also irregular. When using a high-power density of 1 W/cm^2, significant

change in the structure of porous silicon was observed in terms of pore diameters and shape as shown in figure 3. These changes are due to the speed of the reaction. The higher the density of the power, the faster the chemical reaction with the silicon wafer. This could be attributed to the extra holes reach the surface lead to further dissolving of the silicon and create excessive etching which in turn decrease the thickness and the etching rate. Table (1) gives the calculated porosity and the surface area for different laser power density.
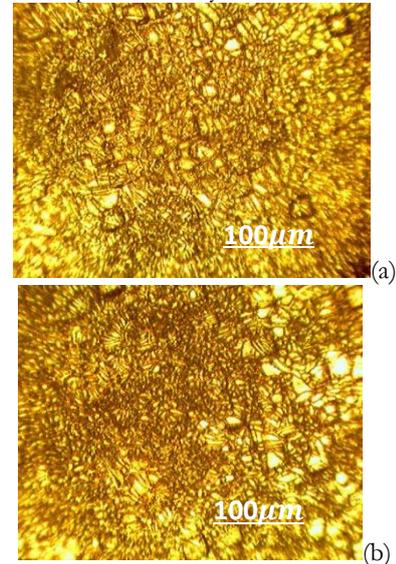
Figure 3: The P-Si surface produce by PEC process using, (a) power density 0.4W/cm^2, (b) power density 0.6 W/cm^2, (c) power density 1W/cm^2.

Table 1: The calculated porosity and surface area for porous silicon prepared by PEC process with different laser power density.

Laser Power density W/cm^2	Porosity %	Surface area (m^2/cm^3)
0.4	85%	340
0.6	90%	410
1	65%	180

The fine features of the upper surface layer of porous silicon can be obtained by atomic force microscopy, an AFM image that gives complete details of the shape and pores diameter with nanoscale dimensions as well as the surface roughness. The samples were examined with different parameters as shown in the following figure 4.

It has been found that the nanostructure synthesized by EC process with current density of $5mA/cm^2$ produces a homogeneous distribution of the nanocrystallie size where the average diameter is 37 nm was used, as show in figure 3. While current density of 10 mA/cm^2 was used small diameter with average value of diameter is 33.71nm is obtained, as show in Figure 4.

Fig 5 demonstrates SEM images for two different EC process samples. A sample prepared with small value of current density $5mA/cm^2$ gives largest surface area and porosity. While for the sample prepared by higher current density $20mA/cm^2$with 30 min time give lower surface area and porosity. The

pore diameters were calculated using the image processing software (image J), figure 6 (left) shows pore size distribution with mean value is about 25 μm. While for the sample prepared with $20\ mA/cm^2$, the pore diameter has more uniform distribution with 32 µm mean value.
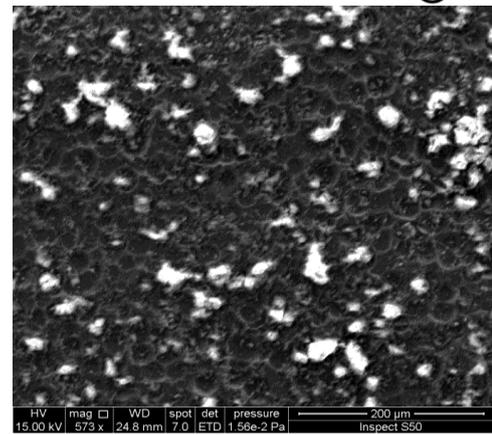
Furthermore, for nanostructure sample prepared by PEC process using laser wavelength of 650 nm produces porous structure of irregular diameters with average value of diameter 42.65nm.

(a)

(b)
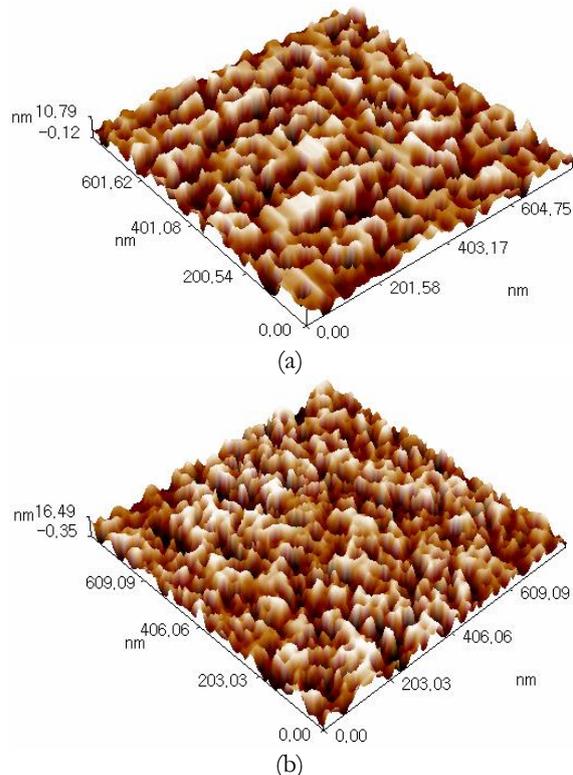
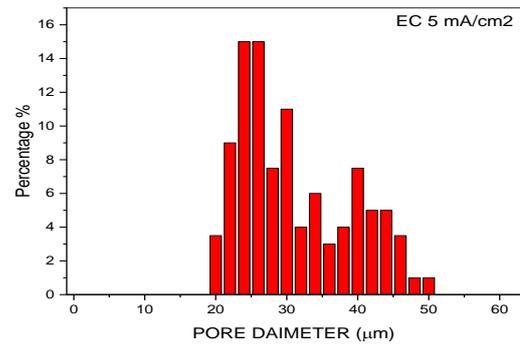**Figure (4):** The AFM images for nanostructured silicon surface produced by 5 and 10 mA/cm² current density.
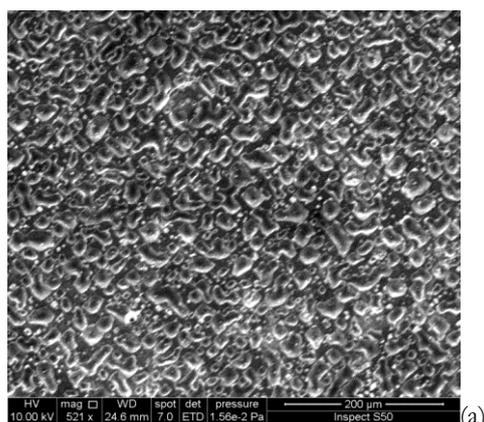
(a)

(b)

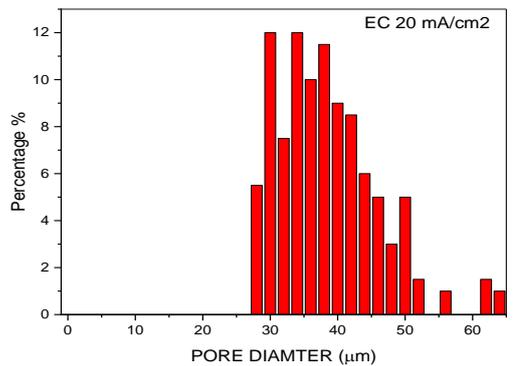**Figure 5:** SEM images for the nanostructured silicon surface prepared by (a) 5 mA/cm² and (b) 20 mA/cm².
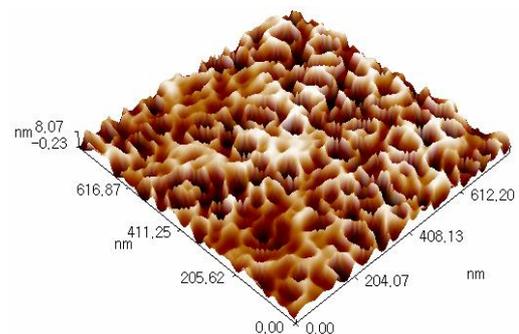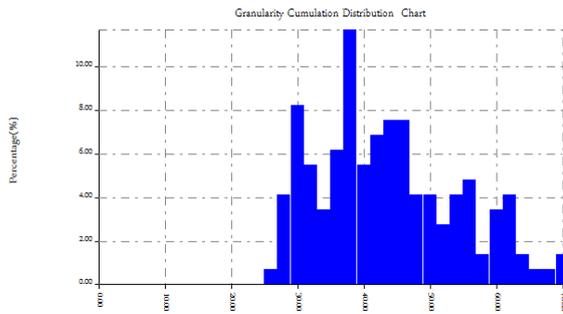

(a)

(b)

Figure 6: The calculated size distribution histograms for the two samples prepared by EC.

Figure (7): The AFM image with size distribution histogram of nanostructured silicon surface prepared by PEC with 650 nm laser beam.

Table 2: Grain size and roughness for different current densities and 650 nm laser wavelength for the sample's investigation in AFM.

Sample	Roughness (nm)	Grain size (nm)
EC, J=$5mA/cm^2$	10.7	37
EC, J=$10mA/cm^2$	16.8	33.71
PEC, $\lambda = 650nm$, J=$20mA/cm^2$	8.3	42.65

The surface resistance and conductivity of the nanostructured silicon samples were measured compared with resistivity about $(0.01-0.02)\Omega.cm$ for silicon wafer. After EC and PEC process, the resistance values increased significantly, as shown in Table 3. The nanostructure surface resistivities were measured using LRC tester for 10 KHz. After embedding the nano silver paste by Nd: YAG laser action with ten number of pulses, 3ms pulse duration and 3J energy, the surface resistivity has decreased drastically to one or two orders of magnitude.

Table 3 shows the resistivity and conductivity values of the nanostructured silicon surfaces processed by PECE and ECE process, with different influencing parameters. It is found that the LIFT process has improved the nanostructured surface resistivity for all samples but the effect was greater for the sample prepared by PEC process compared to EC process and that is due to the effect of PEC process on size reduction and modification the nano silicon surface. Thereby, one can achieve large surface area and a small resistance. Also, one could notice that the resistivity values after the LIFT for the samples produced by ECE process are lower than that for samples prepared PECE process.

Table 3: The surface resistivity and conductivity values of the porous silicon samples with different parameters, before and after the LIFT process.

parameters	ρ	σ	ρ_{LIFT}	σ_{LIFT}
$20mA/cm^2$	2×10^3	5×10^{-4}	1.2×10^2	8.3×10^{-3}
$15mA/cm^2$	3.8×10^3	2.6×10^{-4}	2.5×10^2	4×10^{-3}
$5mA/cm^2$	2.5×10^3	4×10^{-4}	2.2×10^2	4.54×10^{-3}
$0.519\ w/cm^2$	5×10^3	2×10^{-4}	4.6×10^2	2.1×10^{-3}
650nm, $20mA/cm^2$	1.4×10^3	7.1×10^{-4}	3.4×10^2	2.9×10^{-3}
650nm, $15mA/cm^2$	5.3×10^4	1.88×10^{-5}	4.1×10^2	2.43×10^{-3}
532nm, $20mA/cm^2$	1.8×10^3	5.5×10^{-4}	3.9×10^2	2.5×10^{-3}
1064nm, $15mA/cm^2$	4.6×10^4	2.17×10^{-5}	3.8×10^2	2.6×10^{-3}
1064nm, $5mA/cm^2$	5.8×10^4	1.72×10^{-5}	4.5×10^2	2.2×10^{-3}

4. Conclusions

Porous silicon constituting silicon nanostructures can be produced by photoelectrochemical and electrochemical etching of silicon in HF acid. The nanostructured surface features were controlled by various parameters like laser wavelength, laser power density and current density. The electrical properties of silicon nanostructure can be improved by embedding silver nanoparticles through LIFT technology to adopt many optoelectronic applications. This work promotes new technology to obtain silicon surface of high surface area and low resistance.

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